a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein each of said self-locking data bus circuits has upper and lower voltage thresholds that cause respective ones of said self-locking data bus circuits to change states when a level of voltage applied to said respective ones of said self-locking data bus circuits passes through one of said thresholds.

Please add the following new claim:

10. (New) The programmable system according to Claim 8, wherein a ratio between said resistance and an output impedance of said non-clocked, non-inverting amplifier chip is approximately 4 to 1.

REMARKS

The Title of the Invention:

The Title of the Invention has been changed to comply with the suggestion made in Paragraph 1, Page 2 of the Final Office Action of the parent application.

The Drawing Changes:

The objections to Figures 1A and 1B set forth in Paragraph 2 of the Final Office Action of the parent application have been reviewed, and two sheets of corrected informal drawings are

submitted herewith for review by the Examiner. It is submitted that the proposed drawing revisions address and overcome the objections set forth in the Final Office Action of the parent application.

The dashed box for reference numeral 220 now only includes one set of circuit elements 10, 12 and 26. Additionally, while the elements "CPU", "DSP", and "CPLD" have been retained, labels "(DSP CHIP)" and "(OTHER CHIPS)" have been removed.

Moreover, the connections between output gates 20A (Figure 1A), 30 (Figure 1B), and 20A and 30 (Figure 2) have been reconnected on the other sides of the output impedances (labeled "int. imped." in the drawings) of gates 20 and 32 since there is no actual node between a gate and its output impedance, the output impedance shown separated from the gate for analysis purposes only.

In addition, drawing figures 3A-14E have been taken from provisional application serial no. 60/109,951 to which the present application claims priority. Changes have been made in the drawings to make them compatible with the present application. That is, Figures 1, 2 and 3 of provisional application have been relabled as Figures 3A, 3B and 3C. Also, some of the reference numbers have been changed to avoid conflict with reference numbers used in the present application. There is no new matter in these new drawings.

The Amendments to the Written Portion of the Specification:

The objections to the form of the specification set forth in Paragraph 3 of the Final Office Action of the parent application have been reviewed. Each specific objection set forth in the Action has been addressed by amendments to the specification set forth herein.

In addition, relevant portions of provisional application serial no. 60/109,951 to which the present application claims priority have been added to the specification. Changes have been made to this new material to conform with the changes made to the new drawings as describer above.

Care has been taken to avoid the introduction of any new matter into the disclosure.

In view of the present amendments, it is believed that the specification is now in full conformity with all requirements of U.S. Patent Law.

The Rejections Under 35 U.S.C. §112, Second Paragraph:

In Paragraph 5 of the Final Office Action of the parent application, various rejections were set forth regarding the terminology used in Claims 4-9.

Each rejection set forth in Paragraph 5 of the Action has been addressed and, it is submitted, corrected by the claim amendments set forth herein, wherefore reconsideration and withdrawal of the rejections under 35 U.S.C. §112, Second Paragraph is respectfully requested.

The Rejections Based Upon the Prior Art:

In Paragraph 6 of the Action, Claim 4 was rejected under 35 U.S.C. §102(b), based upon U.S. Patent No. 5,230,067 to Buch (hereinafter "Buch").

In Paragraph 7 of the Action, originally submitted Claims 5-9 were rejected under 35 U.S.C. §103(a), based upon Buch.

Request for Reconsideration and Withdrawal of the Prior Art Rejections under 35 U.S.C. §§102(b) and 103(a):

The claims have been amended to add the restriction that circuitry operates in an electrically noisy environment. There is no teaching or suggestion in Buch of using the presently claimed circuit in such an environment. The material added from the provisional application shows that the present application operates in an electrically noisy environment in that driver circuitry for one or more motors, one or more solenoids, one or more relays, and switch sensing circuitry are on the same PC board as the bus using the present invention.

While Buch teaches in paragraph spanning columns 6 an 7 that "The actual value of the [feedback] resistance can fall anywhere between a maximum determined by DC loading of the bus and the need to maintain valid logic states between the drives...." Buch does not contemplate the use of his circuit in a noisy environment. Buch goes on to say "Generally, the resistance value represents some mean value between the output impedance of the drivers and the sum of the input impedances of the various receiver nodes ...

associated with the bus. In TTL Logic systems, this ratio is about 100:1, whereas in CMOS systems, this ratio is about 10,000:1." The mean value would therefore be about 50 times the output impedance of the inverter 66 in a TTL system, and about 5,000 times the output impedance of the inverter 66 in a CMOS system. For an output impedance of inverter 66 of five ohms, for example, in a CMOS system, the feedback resistance would be 250K which does not provide a sufficiently low impedance for dampening noise impressed on the bus. In the present application, which uses CMOS circuits (as indicated by chips 8088 in Figure 8 and 586 in Figure 9) a ration of 4:1 between the feedback resistance and the output impedance on the non-inverting amplifier 20. Thus an amplifier with an output impedance of 5 ohms would have a feedback resistance of 20 ohms, which would provide a substantial dampening effect on electrical noise compared with a feedback resistance of 250K. It is submitted that an electrical noisy environment was not contemplated by Buch.

Independent Claim 4 now recites that the self-locking memory circuit includes a non-clocked, non-inverting amplifier chip for connection to one of the bit lines.

Regarding the rejection of originally submitted Claims 2 and 3 under 35 U.S.C. §103(a), it is noted (e.g., at Page 10, lines 5-9) in the outstanding Action that Buch does not specifically teach the interconnection of a central processing unit with either or both of a Digital Signal Processor and a Complex Programmable Logic Device through a tri state data bus having self-locking data bus

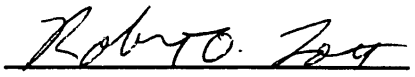
circuits for maintaining the respective bit lines of the tri state data bus in their last driven state, as is presently recited in newly submitted Claims 5, 6, and 8.

It is further respectfully submitted that neither is there any suggestion (to one of ordinary skill in the relevant art) in Buch that a central processing unit could or should be interconnected with either or both of a Digital Signal Processor or a Complex Programmable Logic Device through a tri state data bus having self-locking data bus circuits for maintaining the respective bit lines of the tri state data bus in their last driven state. It is submitted that the proposed modification of the Buch teachings to include the interconnection of a central processing unit with either or both of a Digital Signal Processor and a Complex Programmable Logic Device can only be arrived at through Applicant's own disclosure, and is not either evident or suggested in the Buch reference standing alone.

Accordingly, in view of the present amendments and the above remarks, it is respectfully submitted that the present application is now in condition for allowance, and early action towards that end is respectfully urged.

If, at any time, the Examiner in charge of this application feels that prosecution of this application could be expedited through a telephone interview, the Examiner is invited to contact the undersigned by telephone at (412) 380-0725.

Respectfully Submitted,

By: 

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APPENDIX A

Title of the Invention:

PROGRAMMABLE SYSTEM INCLUDING SELF LOCKING MEMORY CIRCUIT FOR A TRISTATE DATA BUS

In the Specification:

Insert a heading immediately after the Title of the Invention, and before the first full paragraph on Page 1 of the Substitute Specification reading as follows:

CROSS REFERENCE TO RELATED APPLICATIONS

***

First full paragraph after the Title of the Invention on Page 1 of the Substitute Specification:

This application claims priority under 35 U.S.C. §119(e) from [co-pending] Provisional Application Serial No. 60/109,951, filed on November 25, 1998 and entitled "Intelligent Door Controller Unit". This Provisional Application is assigned to Westinghouse Air Brake Company, the assignee of the present application, and is incorporated herein by reference thereto.

***

Paragraph spanning Pages 1 and 2 of the Substitute Specification:

In the above-noted provisional application, a self-locking circuit is shown connected to a tri state bit line of a data bus interconnecting a central processing unit (or "CPU") and other digital transceiving processing devices, such as a Motion Control

Digital Signal Processor (or "DSP"), to provide a memory of the last data value or electrical potential sent on such line, i.e., the last read or write transfer between the CPU and the processing devices. The line is said to be "tri state" because of the three voltage states which the line can assume, namely, a high voltage state, a low voltage state and a state in which no current flow is generated.

***

Second full paragraph on Page 2 of the Substitute Specification:

The present invention uses a known, commercially available, non-inverting, non-clocking buffer amplifier chip and a simple parallel resistor connected across the chip, i.e., connected to the input and output terminals of gates of the chip. These two means (chip and resistor) when connected to a tri state bit line provide a predetermined relatively high impedance on the line that is effective in latching the latest value found on the line.

***

Please replace the first full paragraph in the section entitled "BRIEF DESCRIPTION OF THE DRAWINGS" of the substitute specification to read as follows:

Figures 1A and 1B, taken together, present a schematic diagram showing eight buffer memory latching circuits of a presently preferred embodiment of the invention and their connection to the bit lines of an eight bit data bus.[; and]

***

First full paragraph on Page 6 of the Substitute Specification:

Reference is now made, more particularly, to the drawings. Figures 1A and 1B together show eight buffer memory circuits, generally designated 220, electrically connected, respectively, to eight tri state bit lines 0 through 7 of a data bus 9 interconnected between tranceiving digital components 20 and 30. An example of such an interconnection of components is the central processing unit (or "CPU") 230, the Motion Control Digital Signal [Motion Control] Processor (or "DSP") 320 and the Complex Programmable Logic Device (or "CPLD") 300 interconnected in the read/write manner shown in Figures 7B and 10B of the above incorporated provisional patent application.

***

Paragraph spanning Pages 6 and 7 of the Substitute Specification:

More particularly, circuit 220 of the invention comprises a digital buffer amplifier chip 10 and a parallel resistor 12 connected across the chip 10 such that the input and output terminals 14 and 16 of the chip 10 (only schematically shown in the figures) are connected together by the resistor. Chip 10 is a well known, commercially available, non-inverting digital amplifier having no clocking elements. Its input terminal 14 is connected to a bit line, namely, bit line 4 in Figure 2. As such, in the circuit 220, the signal or potential newly applied to input 14 of

the chip 10 from the bit line is retained after current in the line builds to a predetermined threshold level for circuit 220.

APPENDIX B

4. (Amended) In an electrically noisy environment a [A] self-locking memory circuit for a tri state data bus having multiple bit lines, said self-locking memory circuit comprising:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein said self-locking memory circuit [having] has upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

5. (Amended) In an electrically noisy environment a [A] programmable system comprising:

a central processing unit;

a Digital Signal Processor for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit[;], said Digital Signal Processor and said central processing unit having different clock rates for accessing said tri state data bus; and

[said Digital Signal Processor and said central processing unit having different clock rates for accessing said tri state data bus; and]

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during said access of said tri state data bus by said Digital Signal Processor and said central processing unit at said different rates.

6. (Amended) The programmable system according to Claim 5, wherein said programmable system further [includes] comprises:

a Complex [programmable] Programmable Logic Device for transceiving discrete electrical signals;

[a] wherein said tri state data bus electrically [interconnecting] interconnects said central processing unit, said Digital Signal Processor, and said Complex Programmable Logic Device[;], said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tri state data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus; and

[said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tri state data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus; and]

wherein said programmable system additionally includes self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during [said]

access of said tri state data bus by said Digital Signal Processor, said Complex Programmable Logic Device, and said central processing unit at said different rates.

7. (Amended) The programmable system according to Claim 5, wherein each of said self-locking data bus circuits includes:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein each of said self-locking [memory circuit having] data bus circuits has upper and lower voltage thresholds that cause respective ones of said self-locking [memory circuit] data bus circuits to change states when a level of voltage applied to said respective ones of said self-locking [memory circuit] data bus circuits passes through one of said thresholds.

8. (Amended) In an electrically noisy environment a [A] programmable system comprising:

a central processing unit;

a Complex Programmable Logic Device for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said [Digital Signal Processor] Complex Programmable Logic Device to said central processing unit[;], said Complex Programmable Logic Device and said

central processing unit having different clock rates for accessing said tri state data bus; and

[said Complex Programmable Logic Device and said central processing unit having different clock rates for accessing said tri state data bus; and]

self-locking data bus circuits connected to respective bit lines of said tri state data bus for maintaining said respective bit lines of said tri state data bus in their last driven state during [said] access of said tri state data bus by said Complex Programmable Logic Device and said central processing unit at said different rates.

9. (Amended) The programmable system according to Claim 8, wherein each of said self-locking data bus circuits includes:

a non-clocked, non-inverting amplifier chip for connection to one of said bit lines; and

a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip;

wherein each of said self-locking [memory circuit having] data bus circuits has upper and lower voltage thresholds that cause respective ones of said self-locking [memory circuit] data bus circuits to change states when a level of voltage applied to said respective ones of said self-locking [memory circuit] data bus circuits passes through one of said thresholds.

10. (New) The programmable system according to Claim 8, wherein a ratio between said resistance and an output impedance of said non-clocked, non-inverting amplifier chip is approximately 4 to 1.